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Two-Switch Non-Isolated Step-Up DC-DC Converter

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Abstract

This paper suggests a new non-isolated high voltage gain DC-DC converter with two switches. The proposed two-switch converter has the following characteristics: a high voltage gain, a continuous input current with a small ripple, a reduction in the size of the inductor, and a simple circuit with only a few elements. A theoretical analysis, guidelines for parameter selection, and a comparison with conventional non-isolated high step-up converters are presented. A prototype of 250 W is set up to demonstrate the correctness of the proposed converter. Results obtained from simulations and experiments are presented.

Key words: DC-DC power conversion, High step-up, Non-isolated converter, Two-switch, Z-source converter

I. INTRODUCTION

A high boost DC-DC converter is usually placed in front of an H-bridge inverter to transfer the low voltage from a renewable energy source to the high bus voltage in a grid-connected inverter [1]. Due to its parasitic effects, the traditional boost converter is not desirable for high boost voltage applications. Recently, a number of researchers have found a lot of DC-DC converter structures to achieve a high voltage gain. These structures include both isolated and non-isolated structures. In the case of isolated structures, a step-up transformer is attached between the DC-source and the output. Isolated high step-up converters can be combined with a transformer [2], [3] to obtain a high voltage gain. However, isolated DC-DC converters use a high-frequency transformer with a complex configuration, which results in increased cost.

In the case of non-isolated structures, a lot of researchers have proposed different topologies. Some of these topologies use a coupled inductor while others do not. In order to improve the voltage gain, high boost converters based on coupled inductors are introduced in [4]-[6]. However, the leakage inductance of a coupled inductor is a troubling problem of coupled-inductor-based topologies. By reducing turns ratio of the coupled magnetics, the converter in [7] can improve the voltage gain without core saturation. Since non-coupled inductor converters lack magnetic components, they can have a high voltage gain with a better efficiency and a high power density. The non-coupled inductor converters are designed using the cascaded [8], voltage lift [9], and interleaved [10] techniques. Other topologies use a switched-inductor (SL) [11], switched-capacitor (SC) [12], [13], hybrid SL/SC [14], [15], voltage multiplier cells [16], and an active switch network [17], [18] to achieve a high voltage gain capability with a transformerless structure.

A Z-source network, which combines two capacitors and two inductors linked in an X-form, is employed in DC-DC power conversion. Fig. 1(a) shows the classical Z-source converter (ZSC) in [19], where the source current is discontinuous. A class of quasi-ZSCs is proposed in [20] to achieve a better source current quality. Fig. 1(b) presents the common-ground-based ZSC (CG-ZSC) in [21]. When the Z-source network is linked to the output according to another path, the CG-ZSC achieves a better boost factor when compared to the classical ZSC. ZSC with three networks is introduced in [22] to obtain a high boost factor. However, the volume, weight, price, and loss of the impedance-source based boost DC-DC converters [19]-[22] are increased due to the use of a lot of passive elements. In [23], a coupled-inductor based Y-shape converter is introduced to obtain a high boost ratio. Nevertheless, a voltage spike on the semiconductor

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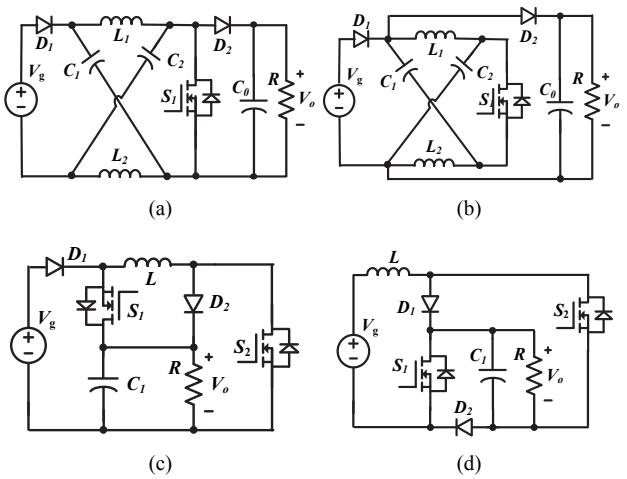


Fig. 1. Z-source and switched-boost DC-DC converters: (a) Classical ZSC [19]; (b) Common grounded ZSC [21]; (c) CIWJ converter [24]; (d) qSBC [25].

devices can occur due to the leakage inductance of the transformer.

Instead of using a single switch and increasing the number of passive components, the inverse Watkins–Johnson (IWJ) converter in [24] uses two switches, an inductor, a capacitor, and two diodes to boost voltage. Fig. 1(c) shows a complementary IWJ (CIWJ) converter. The CIWJ converter has a lower voltage gain when compared with the classical ZSC. In addition, the input current of the CIWJ is discontinuous because it is directly connected to a diode. To improve the negative characteristics of the CIWJ converter, a family of quasi-switched boost converters (qSBCs) was proposed in [25]. Fig. 1(d) presents a qSBC with a continuous input current. However, the voltage stress on the semiconductor devices in the qSBC is equal to the load voltage. Moreover, the voltage boost factor of the qSBC is not large. Therefore, the qSBC has limited application for a high boost voltage gain. A switched-capacitor-based dual-switch high boost converter has been proposed in [26] without reducing the inductor current ripple.

This paper introduces a new high boost DC-DC converter, which uses two switches to reduce the number of passive components. The introduced converter is based on the CIWJ converter topology with the addition of a diode and a capacitor. The major characteristics of the introduced converter are as follows: a high voltage gain, a continuous input current with a small ripple, a reduction in the volume of the inductor, and a simple circuit. The operating principles, analyses in both the continuous conduction mode (CCM) and discontinuous conduction mode (DCM), as well as design guideline of the passive component parameters of the introduced converter are presented. Results from simulations and experiments are presented.

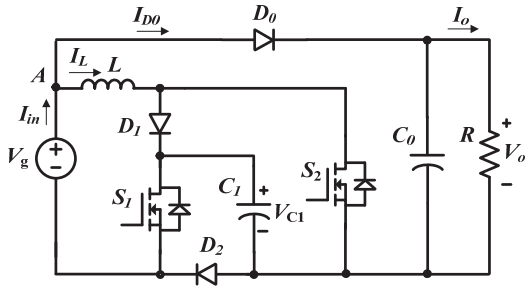


Fig. 2. Proposed two-switch non-isolated high boost converter.

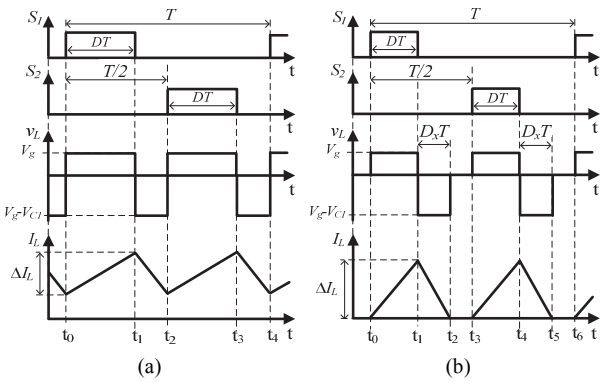


Fig. 3. Typical waveforms in: (a) CCM. (b) DCM.

II. Introduced Two-Switch Non-Isolated DC-DC Converter

Fig. 2 indicates the proposed two-switch non-isolated high step-up converter. This structure includes a boost inductor (L), two capacitors (C_o and C_1), three power diodes (D_0–D_2), two power switches (S_1 and S_2), and a load (R).

Fig. 3 presents typical waveforms of the proposed converter in CCM and DCM operations. The switch S_2 is shifted 180 degrees from S_1. The duty ratio of the switch i.e., D is less than 0.5. As shown in Fig. 3, the operating frequency of the boost inductor is twice the switching frequency. This leads to a decrease in the size of the inductor in comparison to the typical boost converter.

A. CCM Theoretical Analysis

For the ease of the circuit analysis, the following terms are guaranteed: the converter is operating in the CCM; the internal resistance of the inductor is r_L, while the other components are ideal with no losses; the capacitor voltage is constant; and the inductor current rises or falls linearly. Figs. 4(a), 4(b) and 4(c) present the operating states of the proposed converter in the CCM.

Stage 1 [t_0–t_1, Fig. 4(a)]: S_1 is switched "ON" and S_2 is switched "OFF." The inductor stores energy. The diodes D_0 and D_1 are "ON" and the diode D_2 is "OFF". In this state, the "ON" time of S_1 is $D{\cdot}T$, where D is the duty ratio and T is the switching period. Applying Kirchhoff's Current Law (KCL) and Kirchhoff's Voltage Law (KVL) to Fig. 4(a), the following is obtained:

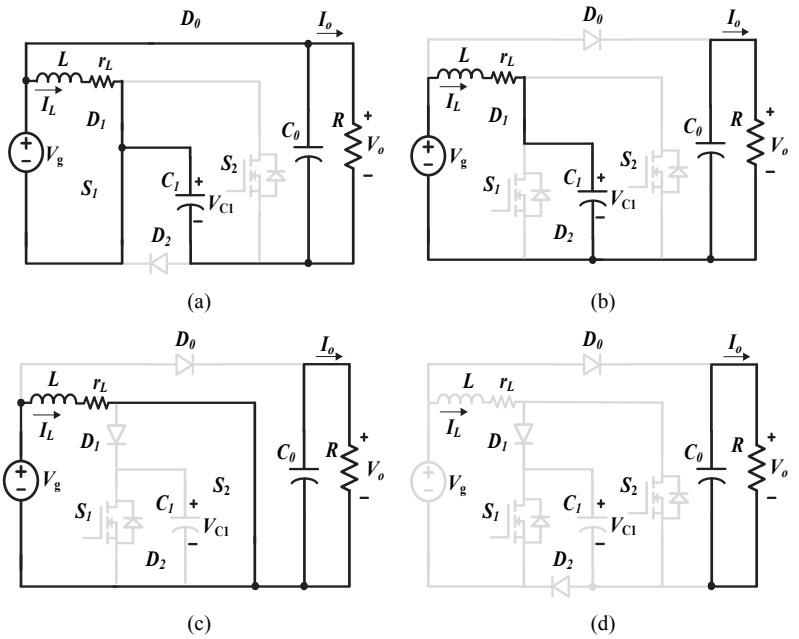


Fig. 4. Equivalent circuits of the proposed two-switch converter with the existence of rL: (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4 in the DCM.

$$\begin{cases} L\dfrac{di_L}{dt} = V_g - r_L I_L \\ V_o = V_g + V_{C1} \end{cases} \text{ and } \begin{cases} C_1\dfrac{dv_{C1}}{dt} = I_L - i_{in\_on} \\ C_0\dfrac{dv_o}{dt} = \dfrac{-V_0}{R} - I_L + i_{in\_on}, \end{cases} \quad (1)$$

where i_{in_on} is the input current during stage 1, when S_1 is turned on.

Stage 2 [t_1–t_2, Fig. 4(b)]: S_1 and S_2 are switched "OFF." The diodes D_1 and D_2 are "ON" and the diode D_0 is "OFF". The time interval in this state is $(0.5 - D)\cdot T$. In this state, the inductor L stores energy and the capacitor C_1 is charged. The following is obtained:

$$L\frac{di_L}{dt} = V_g - V_{C1} - r_L I_L \text{ and } \begin{cases} C_1\dfrac{dv_{C1}}{dt} = I_L \\ C_0\dfrac{dv_o}{dt} = \dfrac{-V_0}{R}. \end{cases} \quad (2)$$

Stage 3 [t_2–t_3, Fig. 4(c)]: S_1 is switched "OFF" and S_2 is switched "ON." The inductor stores energy. The diode D_2 is "ON" and the diodes D_0 and D_1 are "OFF". The time interval in this state is the same as that in state 1. Applying KVL and KCL in Fig. 4(c), the following can be obtained:

$$L\frac{di_L}{dt} = V_g - r_L I_L \quad \text{and} \quad \begin{cases} C_1\dfrac{dv_{C1}}{dt} = 0 \\ C_0\dfrac{dv_o}{dt} = \dfrac{-V_0}{R}. \end{cases} \quad (3)$$

Stage 4 [t_3–t_4, Fig. 4(b)]: This state is the same as stage 2 and its time interval is $(0.5 - D)\cdot T$. In addition, (2) is obtained.

In the steady state the average of the inductor is zero. From (1) to (3), the following can be obtained:

$$V_{C1} = \frac{V_g - r_L I_L}{1-2D},\ i_{in\_on} = \frac{1-D}{D} I_L \text{ and } I_L = \frac{1}{1-2D}\frac{V_o}{R}. \quad (4)$$

Substituting (4) into (1), the output voltage of the proposed converter in the CCM is:

$$V_o = V_g + V_{C1} = \frac{2(1-D)(1-2D)R}{(1-2D)^2 R + r_L} V_g. \quad (5)$$

From (5), the duty cycle D should be lower than 0.5.

B. DCM Theoretical Analysis

The proposed converter enters the DCM when the load resistance is increased to a light load. In the DCM, a larger voltage gain is obtained. Typical waveforms in the DCM are drawn in Fig. 3(b).

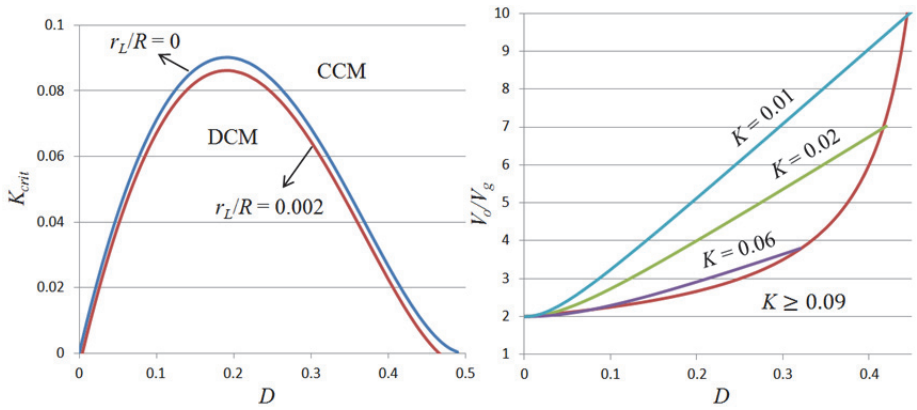
Stage 1 [t_0–t_1, Fig. 4(a)]: This state is the same as stage 1 in the CCM. Based on (1), the peak-to-peak inductor current in state 1 is:

$$\Delta I_L = \left(V_g - r_L I_L\right) DT / L. \quad (6)$$

Stage 2 [t_1–t_2]: An equivalent circuit of this state in the DCM is presented in Fig. 4(b). The time interval in this state is $D_x\cdot T$. The inductor voltage equation is expressed in (2). Stage 2 in the DCM finishes when the inductor current is reduced to zero.

Stage 3 [t_2–t_3, Fig. 4(d)]: S_1 and S_2 are kept "OFF" and no current flows to the inductor. The capacitor C_o is discharged. The inductor voltage in this state is zero.

Stage 4 [t_3–t_4, Fig. 4(c)]: This state is the same as stage 3 in the CCM and its time interval is $D\cdot T$.



(a) (b)

Fig. 5. Relationship between: (a) K_{crit} and D at the CCM/DCM boundary; (b) Voltage gain and D in an ideal case.

Stage 5 [t_4–t_5, Fig. 4(b)]: This state is the same as stage 2 in the DCM. The time interval in this state is $D_x \cdot T$. The inductor voltage is calculated using (2). Stage 5 in the DCM finishes when the inductor current is reduced to zero.

Stage 6 [t_5–t_6, Fig. 4(d)]: This state is the same as stage 3 in the DCM.

According to Fig. 3(b), the average value of the inductor current is determined as:

$$\bar{I}_L = \Delta I_L \left(D + D_x\right) = \frac{V_g - r_L I_L}{L} D\left(D + D_x\right) T. \tag{7}$$

In the DCM in the steady state, the following can be obtained:

$$D_x = \frac{D(V_g - r_L I_L)}{V_{C1} - V_g + r_L I_L}. \tag{8}$$

Assuming that the power loss of the circuit is zero, the following equation can be obtained:

$$\bar{I}_{in} = \frac{P_o}{V_g} = \frac{V_o^2}{R V_g}, \tag{9}$$

where P_o, $\bar{I}_{in}$ and V_o are the load power, the average value of the input current, and the output voltage, respectively.

Applying KCL at node A in Fig. 2, the following can be obtained:

$$\bar{I}_L = \bar{I}_{in} - \bar{I}_{D0}, \tag{10}$$

where $\bar{I}_{D0}$ is the average current of the diode D_0.

Since the average value of the capacitor C_o current does not appear, the average current of the diode D_0 is the load current. From (9) and (10), the average value of the inductor current is:

$$\bar{I}_L = \frac{V_o^2}{V_g R} - \frac{V_o}{R}. \tag{11}$$

The operating condition in the DCM is:

$$\bar{I}_L < \Delta I_L / 2. \tag{12}$$

Substituting (6) and (11) into (12), the following can be obtained:

$$K < K_{crit}(D), \tag{13}$$

where $K = 4L/(RT)$ and $K_{crit}(D) = D \cdot (1–2D)^2/(1–D)–2r_L/R$.

Based on (7), (8), and (11), the voltage gain in the DCM is calculated as:

$$V_o / V_g = \frac{(1-2D)Rk - 2D^2 r_L}{\left[(1-2D)R + r_L\right]k} + \sqrt{\frac{\left[(1-2D)Rk - 2D^2 r_L\right]^2}{\left[(1-2D)R + r_L\right]^2 k^2} + \frac{4(1-2D)D^2 R}{\left[(1-2D)R + r_L\right]k}}. \tag{14}$$

In the ideal case (r_L = 0), (14) is simplified as $1 + \sqrt{1 + 4D^2 / K}$.

The relationship between K_{crit} and D at the CCM/DCM boundary is drawn in Fig. 5(a). In the case of $K < K_{crit}$, the operating region of the converter is the DCM. The relationship between G and D in the ideal case (r_L = 0) is drawn in Fig. 5(b). The value of G in the CCM is smaller than that of the DCM. In case of $K \geq 0.09$, the operating region of the converter is the CCM.

C. Small Signal Analysis

The state-space averaging method is used to derive a small signal analysis of the proposed converter in the CCM. The state variables are $i_L(t)$, $v_{C1}(t)$, and $v_o(t)$, while the input variable is $v_g(t)$. From Fig. 3(a), the differential equations for stage 1 are:

$$\begin{cases} L \dfrac{di_L(t)}{dt} = v_g(t) \\ C_1 \dfrac{dv_{C1}(t)}{dt} = i_L(t) - i_{in\_on} \\ C_0 \dfrac{dv_o(t)}{dt} = \dfrac{-v_0(t)}{R} - i_L(t) + i_{in\_on}. \end{cases} \tag{15}$$

The differential equations for stage 2 in Fig. 3(b) are:

$$\begin{cases} L\dfrac{di_L(t)}{dt} = v_g(t) - v_{C1}(t) \\ C_1\dfrac{dv_{C1}(t)}{dt} = i_L(t) \\ C_0\dfrac{dv_o(t)}{dt} = \dfrac{-v_0(t)}{R}. \end{cases} \quad (16)$$

The differential equations for stage 3 in Fig. 3(c) can be written as:

$$\begin{cases} L\dfrac{di_L(t)}{dt} = v_g(t) \\ C_1\dfrac{dv_{C1}(t)}{dt} = 0 \\ C_0\dfrac{dv_o(t)}{dt} = \dfrac{-v_0(t)}{R}. \end{cases} \quad (17)$$

Applying small-signal perturbations to the average variable, the small-signal relationships among the state variables can be deduced. From (15)–(17), the state space averaged model is:

$$\begin{cases} sL\hat{i}_L(s) = \hat{v}_g(s) - (1-2D)\hat{v}_{C1}(s) + 2V_{C1}\hat{d}(s) \\ sC_1\hat{v}_{C1}(s) = (1-D)\hat{i}_L(s) + \dfrac{1}{D}\hat{d}(s) \\ sC_0\hat{v}_o(s) = \dfrac{(1-2D)I_L}{D}\hat{d}(s) - \dfrac{\hat{v}_0(s)}{R} - D\hat{i}_L(s). \end{cases} \quad (18)$$

Simplifying (18), the control-to-output–voltage transfer function of the proposed converter is obtained as (19).

$$Gvd(s) = \left.\frac{\hat{v}_o(s)}{\hat{d}(s)}\right|_{\hat{v}_g(s)=0} = \frac{b_0 s^2 + b_1 s + b_2}{a_0 s^3 + a_1 s^2 + a_2 s + a_3}. \quad (19)$$

where $a_0 = LC_1C_0$, $a_1 = LC_1/R$, $a_2 = (1-D)(1-2D)C_0$, $a_3 = (1-D)(1-2D)/R$, $b_0 = (1-2D)LC_1I_L/D$, $b_1 = -2DC_1V_{C1}$, and $b_2 = (1-D)(1-2D)^2I_L/D + 1 - 2D$.

III. Passive Element Selections

A. Inductor Design

The inductor is designed according to the peak-to-peak current ripple as calculated in (6). If $\Delta I_L < a\%I_L$, the required inductance in the CCM should be:

$$L > L_{crit} = \frac{2D(1-D)TV_g^2}{a\%P_o}, \quad (20)$$

where L_{crit} is the critical inductance of the proposed converter. The required inductance in the DCM is $L < L_{crit}$.

B. Capacitor Design

The capacitor values are selected based on the capacitor voltage ripple. The capacitor C_1 current in stage 2 of the converter, in Fig. 4(b), is equal to the inductor current as:

$$C_1\frac{\Delta V_{c1}}{(0.5-D)T} = I_L. \quad (21)$$

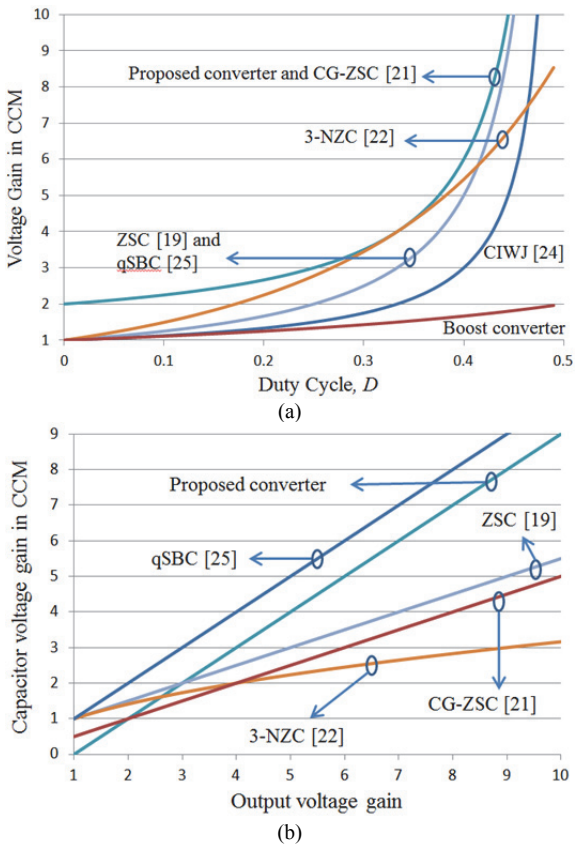


Fig. 6. Voltage gain comparisons in the CCM: (a) Output voltage gain vs. duty cycle; (b) Capacitor voltage gain vs. output voltage gain.

With the capacitor voltage ripple limited by b%, the capacitor value of C_1 in the CCM of the proposed converter is determined as:

$$C_1 > C_{1\_crit} = \frac{(0.5-D)(1-2D)TP_o}{2b\%(1-D)V_g^2}, \quad (22)$$

where C_{1_crit} is the critical capacitance of C_1.

When S_1 is turned off, the output capacitor C_0 current is equal to the load current as:

$$C_0\frac{\Delta V_o}{(1-D)T} = \frac{P_o}{V_o}. \quad (23)$$

If the ripple of the output voltage is limited by c%, the capacitance of C_0 in the CCM should be:

$$C_0 > C_{0\_crit} = \frac{(1-2D)^2TP_o}{4c\%(1-D)V_g^2}, \quad (24)$$

where C_{0_crit} is the critical capacitance of C_0.

The required C_1 and C_0 capacitances in the DCM are $C_1 < C_{1\_crit}$ and $C_0 < C_{0\_crit}$, respectively.

C. Input Current Ripple

According to Fig. 4, the source current is i_{in_on} in state 1, and it is equal to the inductor current in states 2 and 3. i_{in_on}

and I_L are calculated as (4). Thus, the peak-to-peak source current ripple is:

$$\Delta I_{in} = \left| i_{in\_on} - I_L \right| = V_o / \left(R \cdot D \right). \quad (25)$$

From (25), it can be observed that the peak-to-peak source current ripple is reduced when the duty ratio is high.

IV. Comparison Study

Table I is presented in order to compare the proposed converter with other non-isolated converter structures. Fig. 6 compares the voltage gains of non-isolated high boost converters in the CCM.

With the Z-source converters in [19] and [22], the proposed two-switch converter adds one switch and uses fewer passive components to achieve a higher voltage gain with low voltage ratings on the components. When compared to the CG-ZSC in [21], the proposed two-switch converter adds one switch and one diode. However, it subtracts one inductor and one capacitor. The proposed two-switch converter has a smaller source current ripple and the same voltage gain as the CG-ZSC. Fig. 6(b) shows the relationship between the voltage gain of the capacitors in the impedance network and the output voltage gain. The capacitor voltage stress of the 3-Z-network converter (3-ZNC) is the lowest. Since the proposed converter only applies one capacitor to the Z-source network, the capacitor voltage stress of the proposed converter is larger than that of both the ZSC and the CG-ZSC, where two capacitors are used in the impedance network. Note that there is only one capacitor in the impedance network of the proposed converter, while there are two in the ZSC and the CG-ZSC.

When compared to the qSBC in [25], the voltage gain of the proposed two-switch converter is higher for the same duty ratio. Moreover, the voltage ratings of the diodes and switches of the proposed two-switch converter are lower than those of the qSBC. As shown in Fig. 3, the inductor operating frequency of the proposed two-switch converter is twice the switching frequency, while the inductor operating frequency of the qSBC is the same as the switching frequency due to the fact that both of the switches in [25] are turned on at the same time in one switching period. As a result, the inductance value in the proposed converter is half that in the qSBC [25]. Table II compares the current stresses of the proposed two-switch converter with those of the qSBC [25]. Because the duty ratio of the proposed converter is less than 0.5, the current stress on the switch S_1 of the qSBC is lower than that of the proposed converter. Therefore, the proposed converter is highly inadvisable when the duty ratio is lower than 0.1. However, the current stresses on the inductor, the switch S_2, and the diodes D_1 and D_2 of the proposed converter are lower than those of the qSBC.

TABLE I
Comparison with Other Boost DC-DC Converters

	ZSC	CIWJ	qSBC	3-ZNC	CG-ZSC	Proposed converter
Ind.	2	1	1	4	2	1
Cap.	3	1	1	2	3	2
Diode	2	2	2	9	2	3
Switch	1	2	2	1	1	2
Switch voltage	V_o	V_o	V_o	V_o	$V_o - V_g$	$V_o - V_g$
Main diode voltage	V_o	V_o	V_o	$\frac{D(1+D)V_o}{\frac{V_o(1-D)}{1+D}}$	$V_o - V_g$	$V_o - V_g$
Output diode voltage	V_o	*NA*	*NA*	V_o	$V_o - V_g$	$V_o - V_g$
Cap. voltage	$\frac{V_o + V_g}{2}$	V_o	V_o	$\frac{V_o(1-D)}{1+D}$	$V_o/2$	$V_o - V_g$
Voltage gain, G	$\frac{1}{1-2D}$	$\frac{1-D}{1-2D}$	$\frac{1}{1-2D}$	$\left(\frac{1+D}{1-D}\right)^2$	$\frac{2(1-D)}{1-2D}$	$\frac{2(1-D)}{1-2D}$
Inductance	$\frac{D(1-2D)TR_L}{2(1-D)a\%}$	$\frac{(1-D)TR_L}{a\%}$	$\frac{2V_g^2(1-D)DT}{a\%(1-2D)P_o}$	$\frac{V_g(1-D)^2}{a\%(1+D)} \times \frac{DT}{I_o}$	$\frac{V_g(1-D)}{a\%I_o} \times \frac{DT}{\left(2-5D+4D^2\right)}$	$\frac{2D(1-D)TV_g^2}{a\%P_o}$
Capacitance	$\frac{DTV_o}{2b\%R_L}$	$\frac{DTP_o}{b\%V_o^2V_g} \times \left(V_o - V_g\right)$	$\frac{P_o(1-2D)DT}{b\%V_g^2}$	$\frac{2I_o}{b\%(1+D)} \times \frac{DT}{V_g}$	$\frac{3-7D+4D^2}{b\%(1-D)} \times \frac{DTI_o}{V_g}$	$\frac{(0.5-D)T}{2b\%(1-D)} \times \frac{(1-2D)P_o}{V_g^2}$
Input current	*Dis.*	*Dis.*	*Cont.*	*Cont.*	*Dis.*	*Cont.*
Current ripple	*High*	*High*	*Low*	*Low*	*High*	*Low*

TABLE II
Current Stress Comparison between the Proposed Converter and the qSBC

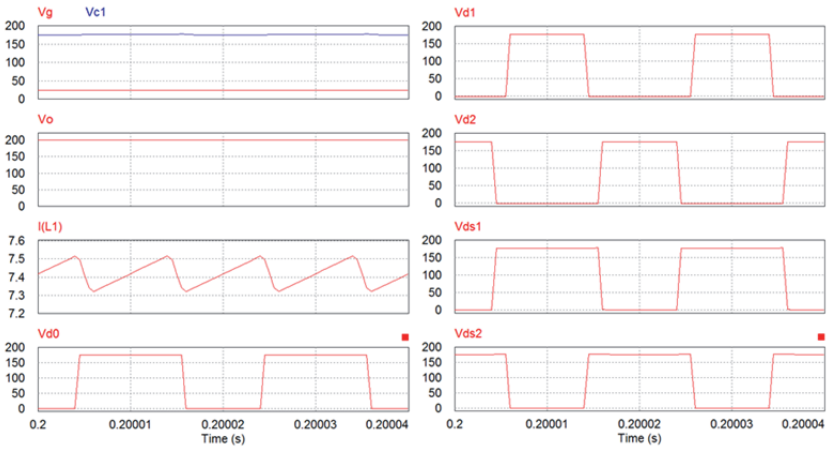
	I_L	I_{S1}	I_{S2}	I_{D1}	I_{D2}	I_{D0}
qSBC [25]	P_o / V_g	P_o / V_g	P_o / V_g	P_o / V_g	P_o / V_g	-
Proposed converter	$\frac{0.5P_o}{(1-D)V_g}$	$\frac{0.5P_o}{DV_g}$	$\frac{0.5P_o}{(1-D)V_g}$	$\frac{0.5P_o}{(1-D)V_g}$	$\frac{0.5P_o}{(1-D)V_g}$	$\frac{0.5P_o}{D(1-D)V_g}$

where I_{S1}, I_{S2}, I_{D1}, I_{D2} and I_{D0} are the peak currents of the switches and diodes.

V. Simulation and Experimental Verifications

A. Simulation Verifications

The proposed converter was verified using PSIM simulation software. Table III lists the simulation parameters of the proposed converter. Figs. 7(a) and 7(b) present simulation verifications of the proposed converter when the input DC source is 25 V. As presented in Fig. 7(a), the voltage of the capacitor C_1 is stepped-up to 175 V. The output voltage of 200 V is the total of the voltage of the capacitor C_1 and the source voltage. The source current is drawn continuously. Fig. 7(c) shows simulation waveforms with an input DC source change. In Fig. 7(c), the load voltage is maintained at 200 V while the source voltage is adjusted from 25 V to 50 V.



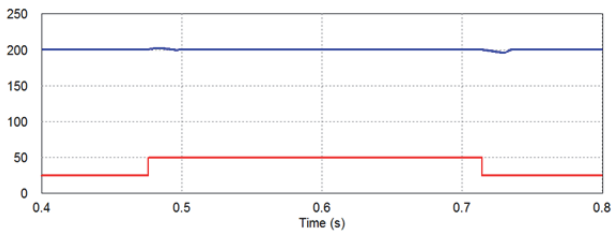


Fig. 7. Simulation waveforms of the proposed converter when: (a) and (b) V_g = 25 V; (c) Input DC source change.

TABLE III
SIMULATION AND EXPERIMENTAL PARAMETERS

Parameters		Values
Source voltage (V_g)		25 V–50 V
Load voltage (V_o)		200 V
Maximum load power (P_o)		250 W
Inductor (L)		1 mH
Capacitors	C_1	3.3 µF/ 305 V (PILKOR)
	C_0	110 µF/ 450 V (PILKOR)
Switching frequency (f_{sw})		50 kHz
MOSFETs	S_1, S_2	IRFP4868PbF
Diodes	D_0, D_1, D_2	FF60UP30DN

The curved shapes of the graph in Fig. 7(a) are the source and capacitor C_1 voltages, the load voltage, the inductor current, and the voltage of the diode D_o, respectively. In Fig. 7(b), the curved shapes are the voltages of the diodes D_1 and D_2 and the drain-source voltages of S_1 and S_2, respectively. In Fig. 7(c), the top curve is the load voltage, while the bottom curve is the source voltage.

B. Experimental Verifications

A laboratory prototype of 250 W was constructed as shown in Fig. 8 to verify the proposed converter. The experimental parameters are listed in Table II. The switching period is 20 µs. The DC source voltage is generated by a programmable AC/DC power supply ES 2000S (NF Corporation), and is adjusted from 25 V to 50 V. The output voltage is 200 V.

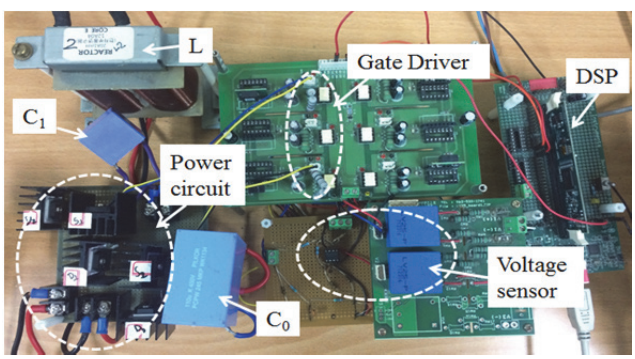


Fig. 8. Experimental prototype.

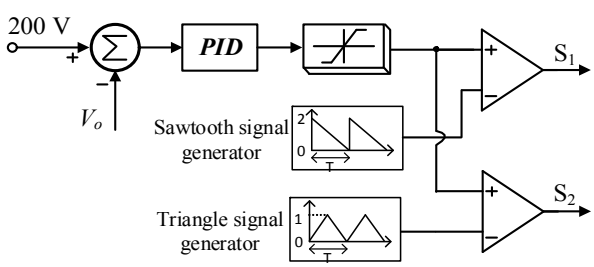


Fig. 9. PID controller algorithm.

Two PWM control signals are generated by a DSP TMS320F28335 microcontroller through isolated amplifiers (TLP250). This is done to drive two MOSFETs. The two switches are IRFP4868PbF and the three diodes are FF60UP30DN. A simple PID controller, as presented in Fig. 9, was applied to the experimental setup to keep the load

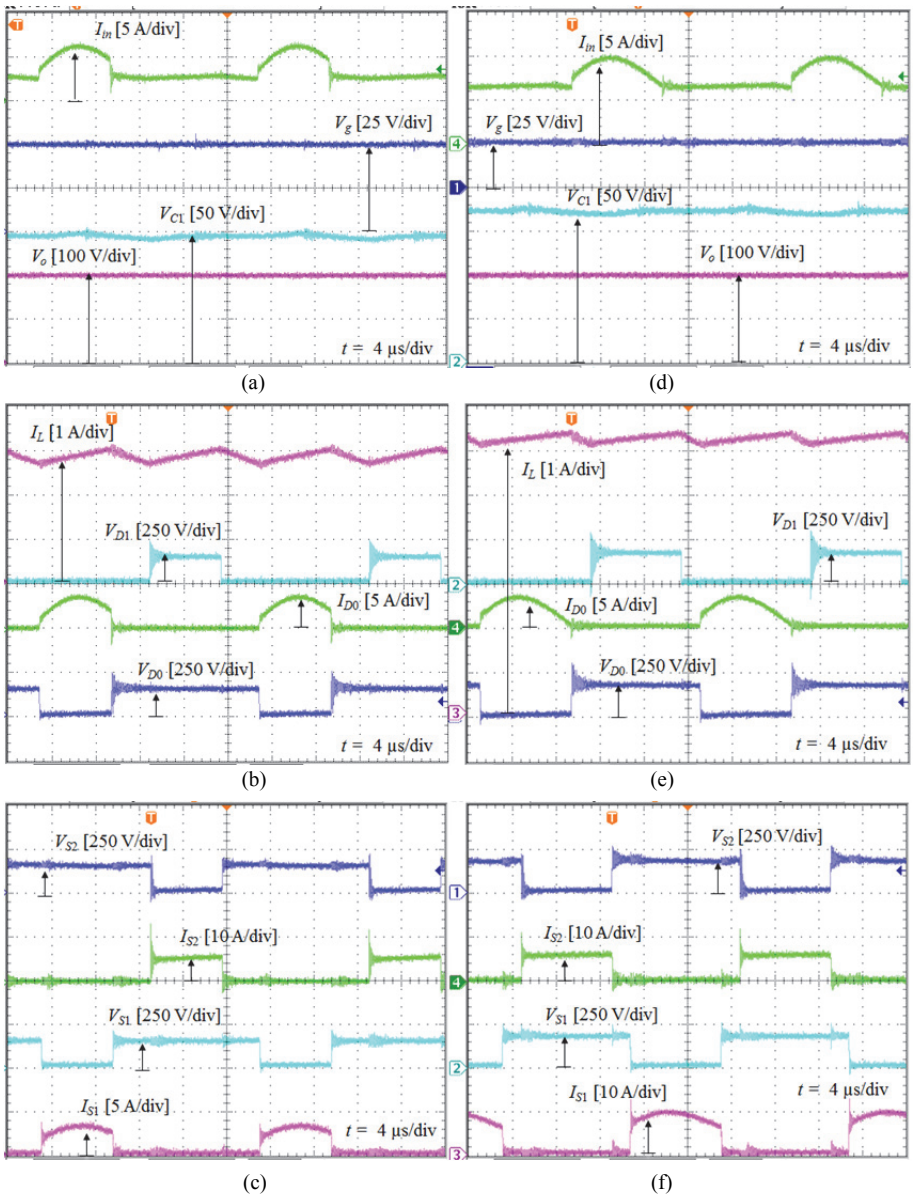


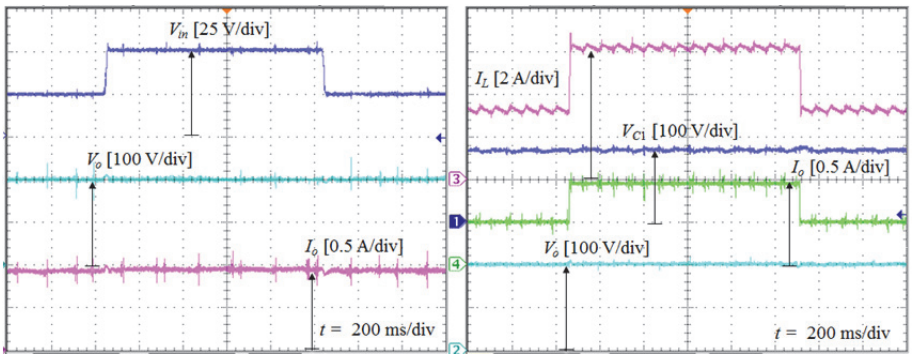
Fig. 10. Experimental waveforms of the proposed converter when: (a)-(c) V_g = 50 V; (d)-(f) V_g = 25 V. (a) and (d) Source current, source voltage, capacitor C_1 voltage, and load voltage; (b) and (e) Inductor current, diode D_1 voltage, diode D_0 current, and diode D_0 voltage; (c) and (f) Voltage and current stresses of S_1, and voltage and current stresses of S_2.

voltage at 200 V. The parameters of the PID controller were determined based on the Ziegler-Nichols tuning method [27].

The proposed converter was verified in the CCM at a load power of 195 W. Fig. 10 presents experimental waveforms of the proposed converter when V_g = 50 V and 25 V. The source current is drawn continuously. When the switch S_1 is conducted, the source current increases. Furthermore, when the switch S_1 is not conducted, the source current decreases. As shown in Figs. 10(a) and 10(d), the measured capacitor C_1 voltages are stepped-up to 150 V and 174 V, respectively. The load voltage in both cases is 200 V.

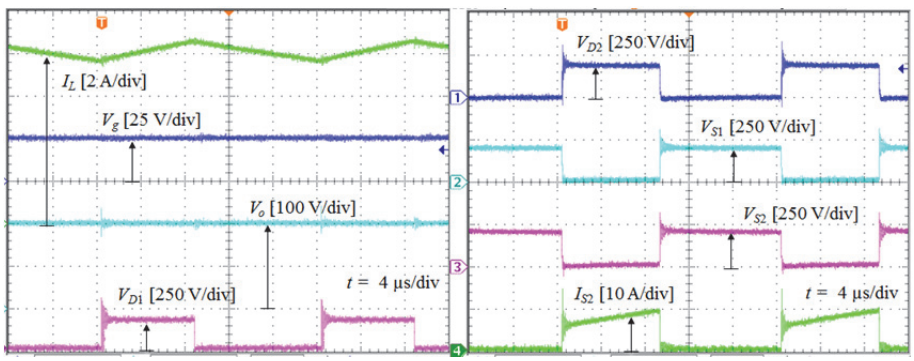
Fig. 11 presents experimental waveforms of the proposed converter when a PID controller is used. In Fig. 11(a), the source voltage is varied from 25 V to 50 V while the load is fixed at 195 W. In Fig. 11(b), the input voltage is maintained at 25 V, while the load power is varied from 99 W to 195 W. In Fig. 11, it is evident that the load voltage is maintained at 200 V, despite the fact that the source voltage or the load is varied. From (25), the peak-to-peak ripple of the input current is increased when the duty cycle is low. Therefore, the proposed converter is highly inadvisable when the duty ratio is low. Because the proposed converter aims at a high voltage gain, the advisable operating area of the duty cycle is in the range of [0.3, 0.44].

The proposed topology is compared with the qSBC in [25]. Fig. 12 shows experimental results of the qSBC when V_g = 25 V, V_o = 200 V and P_o = 195 W. In this experiment, the parameters shown in Table III are used in the qSBC. When



(a) (b)

Fig. 11. Experimental waveforms with: (a) Source voltage change from 25 V to 50 V; (b) Load change from 99 W to 195 W. (a) Source voltage, load voltage, and output current; (b) Inductor current, capacitor C_1 voltage, output current, and output voltage.



(a) (b)

Fig. 12. Experimental results of the qSBC [25] when: V_g = 25 V, V_o = 200 V, and P_o = 195 W. (a) Source (or inductor) current, source voltage, output voltage, and diode D_1 voltage; (b) Diode D_2 voltage, drain-source voltage of S_1 and S_2, and current of S_2.

comparing the experimental waveforms in Fig. 12 to those in Fig. 10, it can be observed that the voltage and current stresses on the inductor, the switch S_1, and the diodes D_1 and D_2 of the proposed converter are smaller than those of the qSBC.

Fig. 13 shows a comparison of the efficiency between the proposed converter and the qSBC. The measured efficiency of the converter is defined as the ratio between the output power and the input power.

As shown in Fig. 13, the efficiency of the proposed converter is higher than that of the qSBC [25]. This is due to the fact that the proposed converter uses a lower duty ratio to obtain the same voltage gain as the qSBC. Moreover, the current stresses on the inductor, the switch S_2, and the diodes D_1 and D_2 of the proposed converter are lower than those of the qSBC, as shown in Table II. As a result of using a lower duty ratio and a lower current stress, the copper loss of the inductor and the conduction loss of the switches and diodes in the proposed converter are lower than those in the qSBC. The maximum efficiency of the proposed converter is 95.2%. The efficiency of the proposed converter is reduced at a low DC source voltage. In comparison to the qSBC, for the same operating conditions as those in the experiment, it can be seen that the proposed converter has a higher cost, a higher volume, a lower reliability and a higher efficiency.

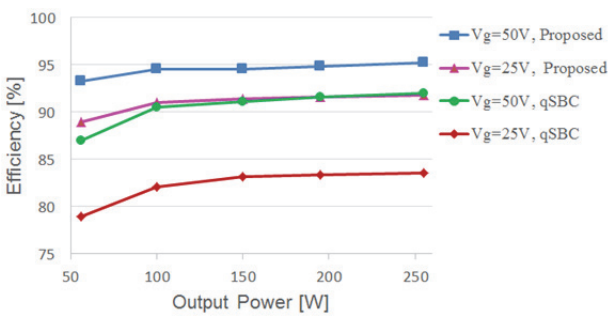


Fig. 13. Efficiency of the proposed converter and the qSBC under various operating conditions.

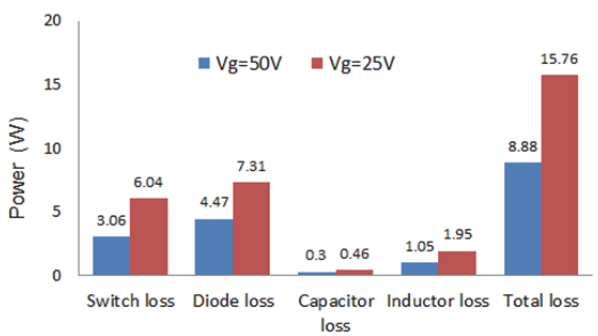


Fig. 14. Calculated losses in the devices at V_o = 200 V, P_o = 195 W, and f_{sw} = 50 kHz.

Fig. 14 shows a loss breakdown in devices with V_o = 200 V, P_o = 195 W, and f_{sw} = 50 kHz. The parameters in Table IV are used to determine of the power losses of the converter in the CCM. As shown in Fig. 14, the capacitor loss is the lowest. When the lowest DC source voltage of 25 V is used, the losses in the MOSFETs and diodes are dominant. The loss determination process of the proposed converter is addressed as follows. First, the conduction current and conduction periods of the devices are determined from the operating states of the proposed converter. Then, the power losses of the switches S_1 and S_2, including the conduction loss and switching loss, are calculated. In addition, the conduction loss and the reverse recovery loss of the diodes are calculated. The capacitor loss is computed based on the equivalent series resistances of the capacitors. Finally, the copper loss and the core loss of the inductor are calculated.

VI. CONCLUSION

In this paper, a new high boost converter with two switches was proposed. The main characteristics of the proposed two-switch converter are its high voltage gain, continuous input current with a small ripple, and simple circuit with only a few passive elements. Theoretical analyses in the CCM and DCM, design guidelines, and comparisons with conventional high boost converters are shown. A 250 W prototype was used to verify the theory. The results obtained from the simulations and experiments match those of the theoretical analysis.

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